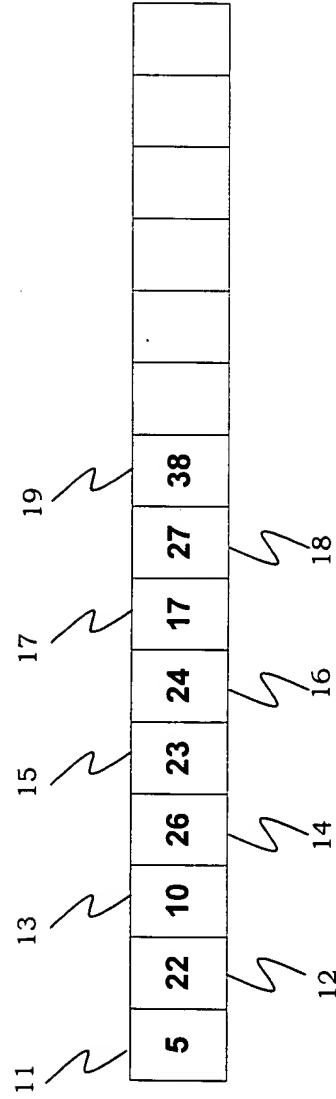


FIGURE 1
(Prior Art)



20

FIGURE 2
(Prior Art)

A) The value in the root node is removed, leaving a "hole".

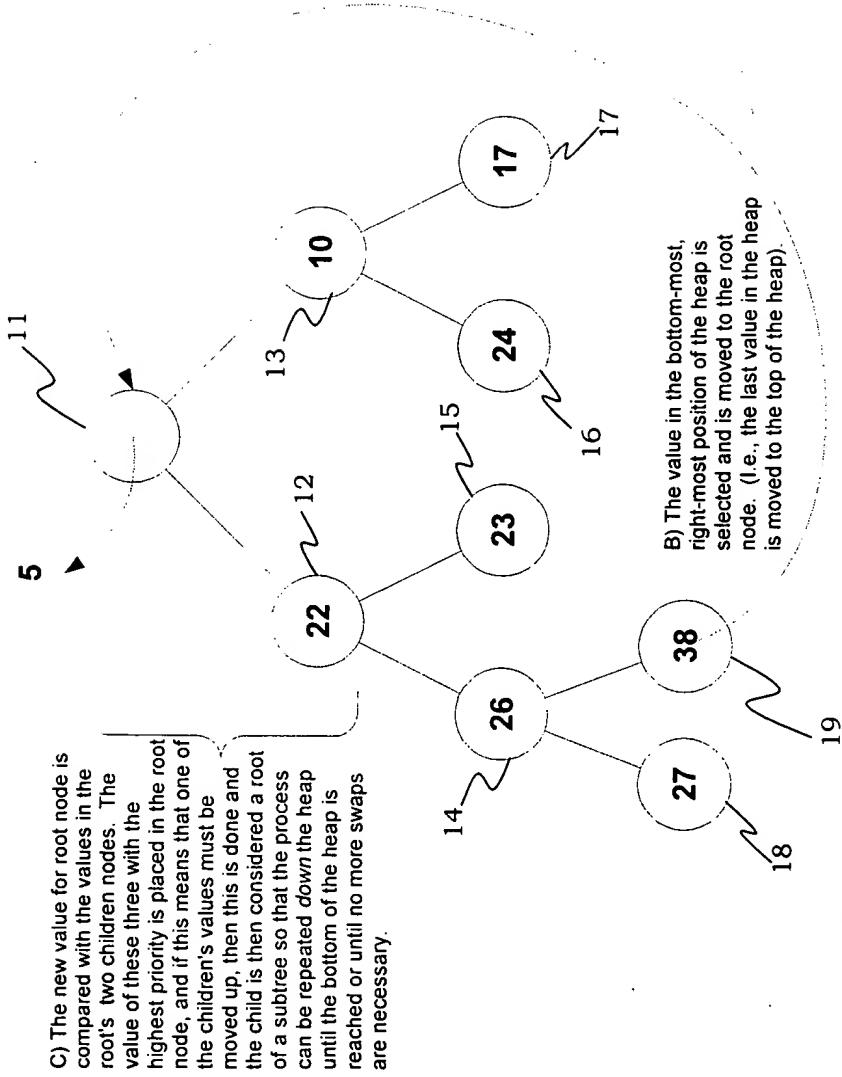


FIGURE 3
(Prior Art)

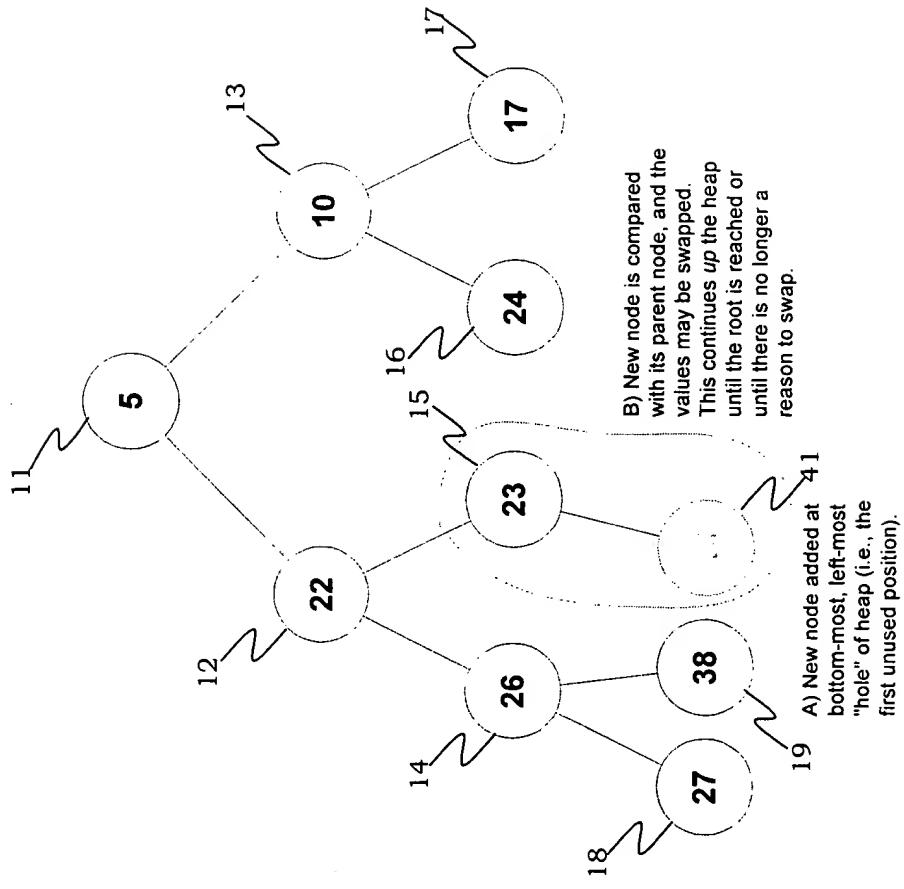
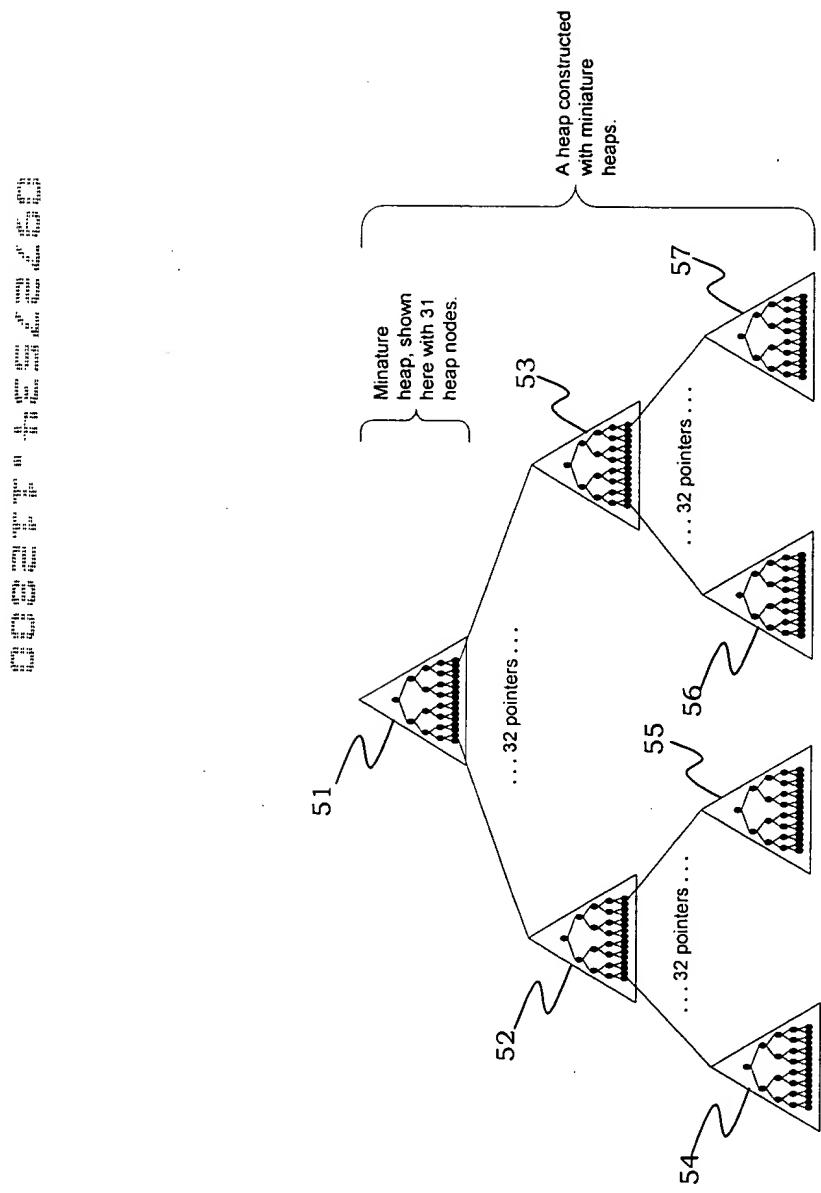


FIGURE 4
(Prior Art)

FIGURE 5



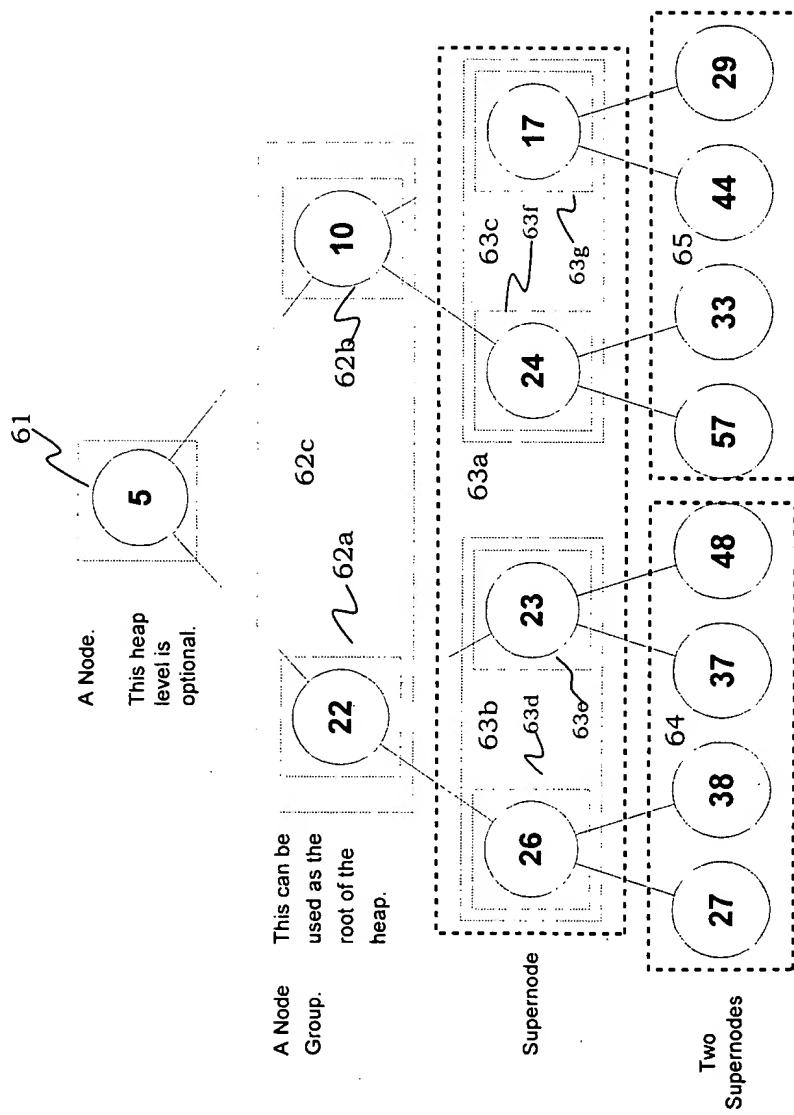
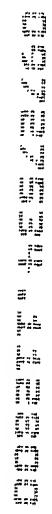


FIGURE 6

Each node is stored in a random memory location -- i.e., the horizontally or vertically adjacent nodes on the diagram are not stored in contiguous memory.

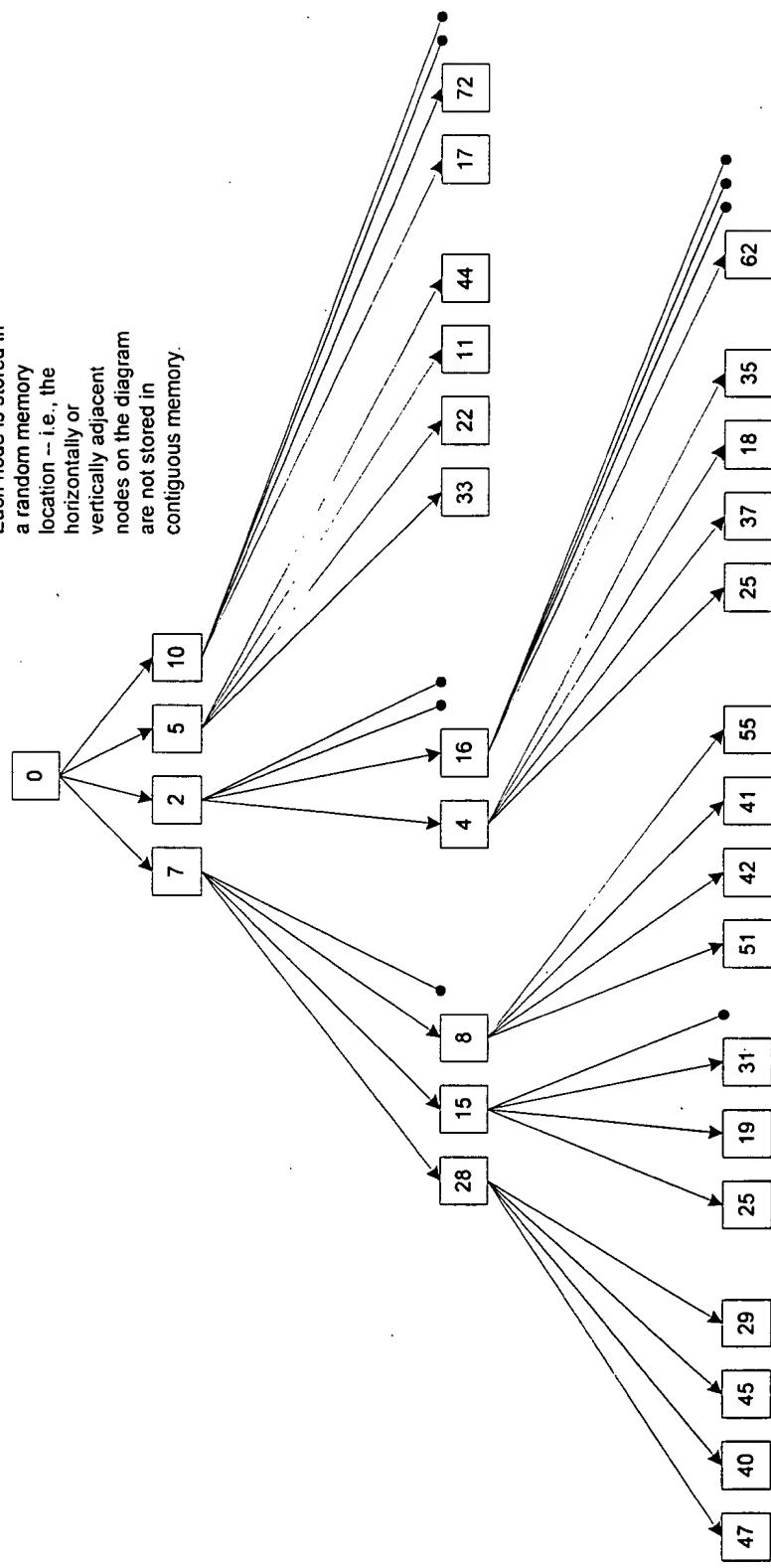


FIGURE 7

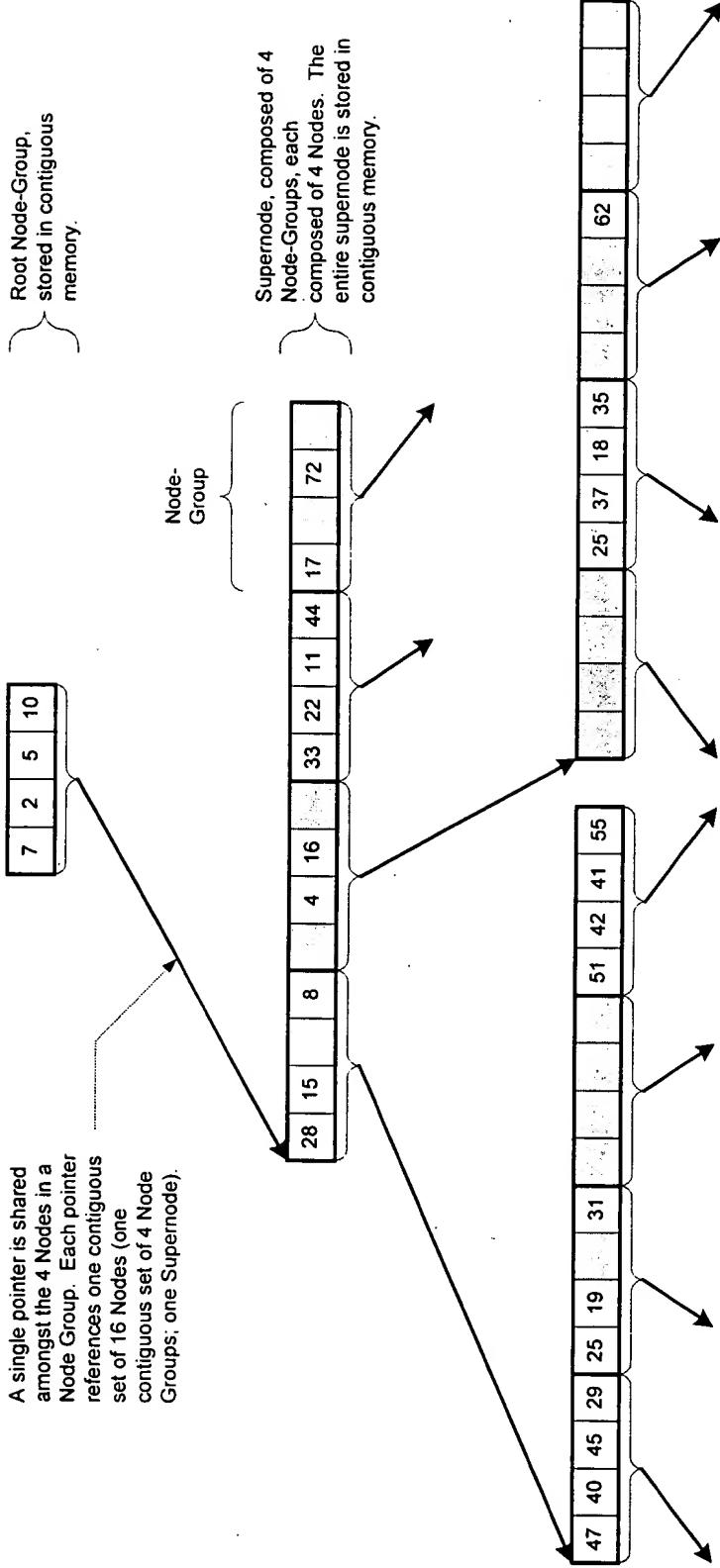


FIGURE 8

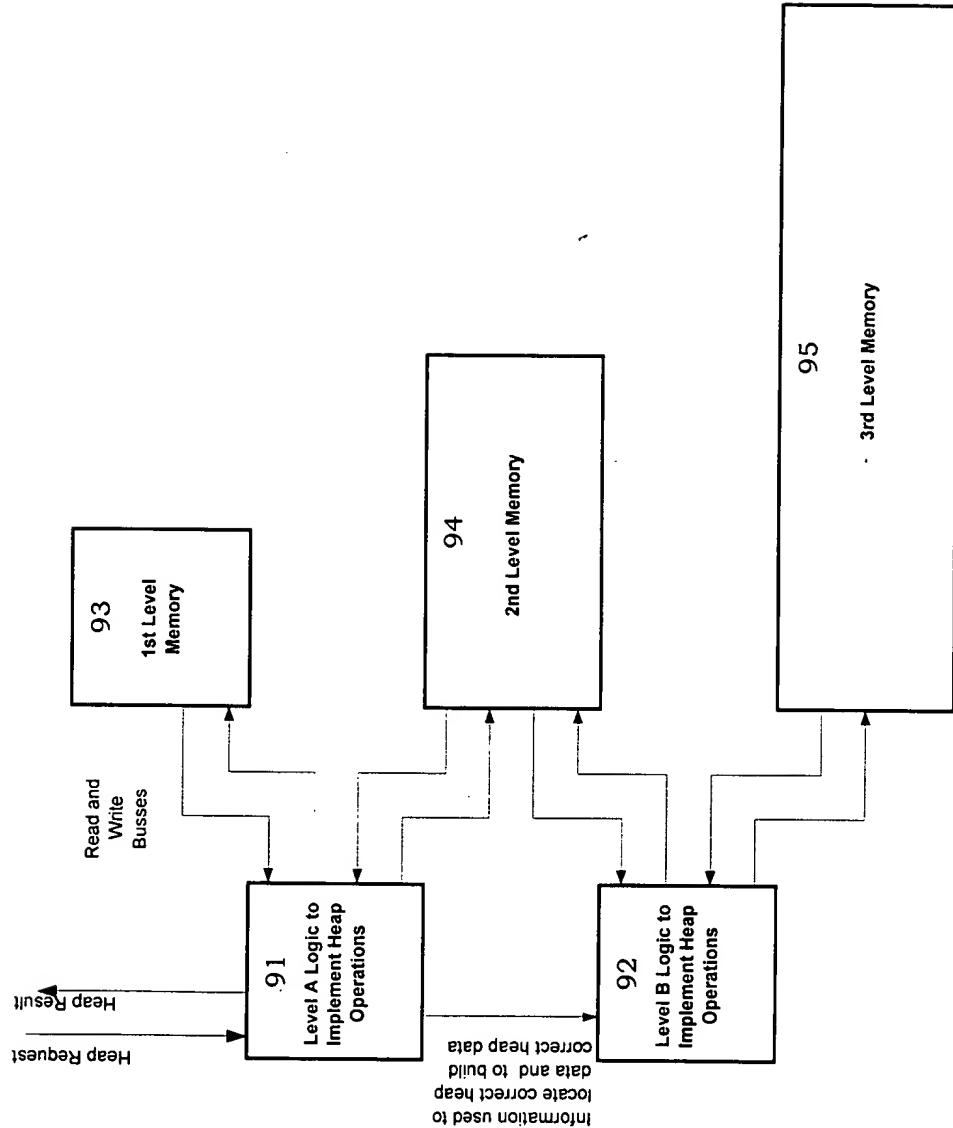


FIGURE 9

0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000

| | time -----> | | | | | | | | | | | | | | | | | |
|----------------------------|-------------|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
| Read Level 1 RAM | A | | | | | B | | | | | | | | | | | | |
| Write Level 1 RAM | | | | | A | | | | | | | | | | | | | |
| Level A Comparisons | | A | A | | | | | | B | | | | | | | | | |
| Read Level 2 RAM | | A | | | | | | B | | | | | | | | | | |
| Write Level 2 RAM | | | | | | A | | | | | | | | | | | | B |
| Level B Comparisons | | | | | A | A | | | | | B | | | | | | B | |
| Read Level 3 RAM | | | | A | | | | | | B | | | | | | | B | |
| Write Level 3 RAM | | | | | | A | | | | | | | | | | | B | |
| Level C Comparisons | | | | | | A | A | | | | | B | | | | B | | |
| Read Level 4 RAM | | | | | | A | | | | B | | | | | | | | |
| Write Level 4 RAM | | | | | | | A | | | | | | | | | | B | |

FIGURE 10

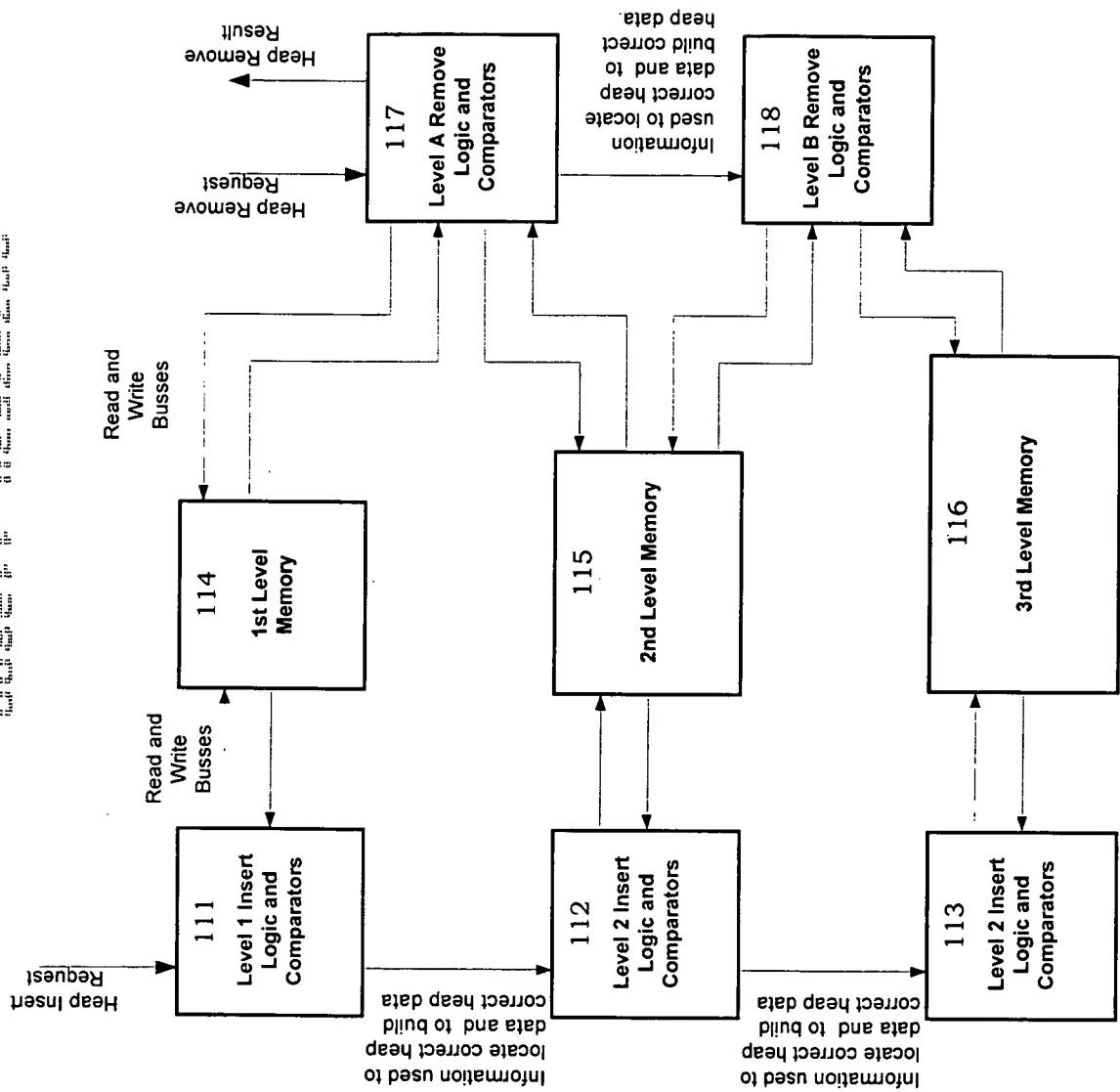


FIGURE 11

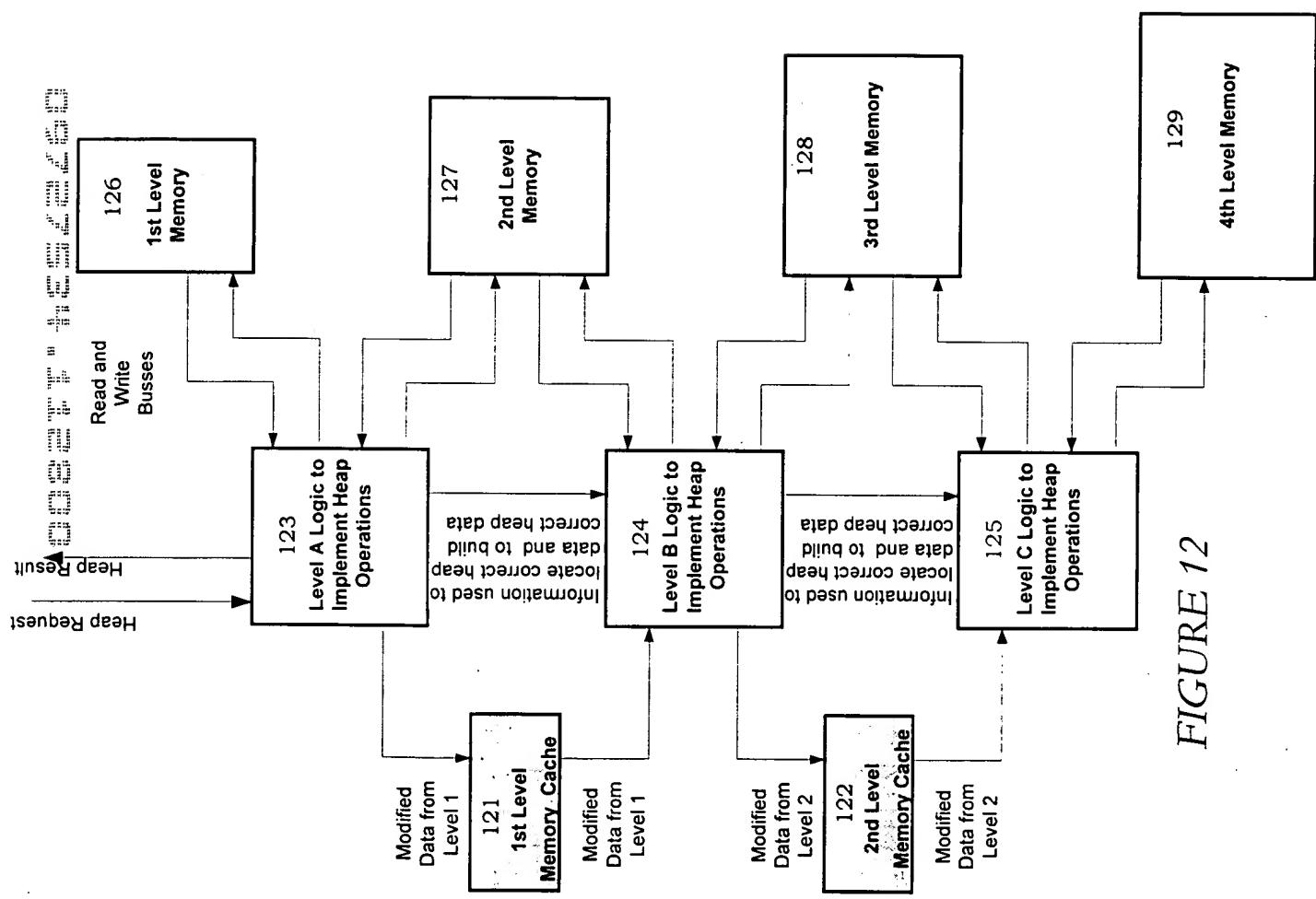


FIGURE 12

| | time | | | | |
|---------------------|------|---|---|---|---|
| Read Level 1 RAM | A | B | C | D | E |
| Write Level 1 RAM | | B | C | D | E |
| Level A Comparisons | A | A | B | C | D |
| Read Level 2 RAM | A | B | C | D | E |
| Write Level 2 RAM | | B | C | D | E |
| Level B Comparisons | A | A | B | C | D |
| Read Level 3 RAM | A | B | C | D | E |
| Write Level 3 RAM | | B | C | D | E |
| Level C Comparisons | A | A | B | C | D |
| Read Level 4 RAM | A | B | C | D | E |
| Write Level 4 RAM | | A | B | C | D |

Diagram illustrating the sequence of memory operations and data consistency across four levels of RAM and four levels of comparisons. The timeline shows the progression of requests A and B. Request A (circled in red) starts at time 1, reads from Level 1 RAM (value A), and is compared at Level A. Request B (circled in red) starts at time 2, reads from Level 1 RAM (value B), and is compared at Level B. The table shows the state of each RAM level at each time step, with values A, B, C, D, or E. The 'Write' row indicates updates to the RAM levels. The 'Level X Comparisons' row shows the results of the comparisons between the RAM values and the current request values (A or B). The 'Read' rows show the values read from the RAM levels at each time step.

Annotations:

- The 2nd request (B) starts to read from level 1 memory. The 1st request (A) starts to modify the data that it read from level one. Thus, if request B reads from the same location as request A, request B will get the old (stale), unmodified data and produce the wrong result.
- Once request A has finished modifying the data that it read, it can write it back. However, it must also cache the data so that when B starts to modify the data that B read, B can discard the data it read and use the current information in the cache instead.
- Request B checks the cache before it modifies the data that it read. If the cache indicates that B is operating on the same memory location in level 1 that request A just operated on, B uses the contents of the cache.

FIGURE 13